Hardware Power Loss Data Protection

Hardware Power Loss Data Protection (HW-PLP) is an efficient method for preventing data loss during sudden power loss events. It is implemented through hardware components in electronic devices and enabled by firmware. HW-PLP utilizes specialized hardware components to detect and respond to power loss events, ensuring that user data is programmed to non-volatile memory before system shutdown. The hardware components used for HW-PLP include capacitors, voltage detectors, along with firmware implementation.

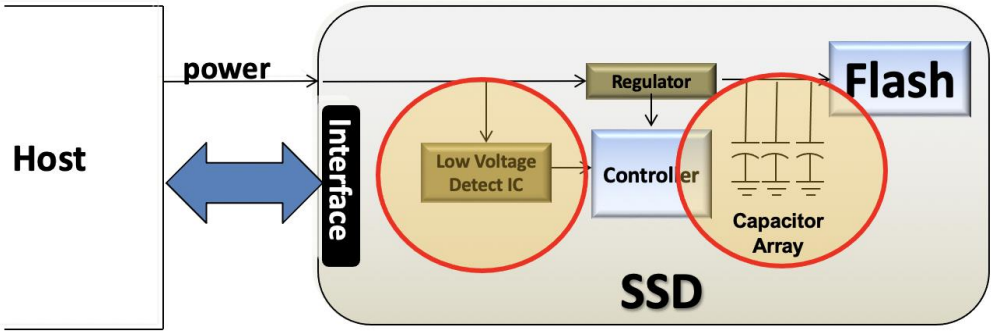

Figure 1 – Hardware implementation of HW-PLP

Hardware Implementation

The voltage detector is the primary component used in HW-PLP. It monitors the voltage level of the power supply to the Flash product and relays the voltage status to the controller CPU. During power loss events, the voltage detector informs the CPU (integrated into the controller) that the voltage has dropped, triggering the firmware process for power loss management.

Capacitors are another key hardware component used in HW-PLP. They store electrical charge and serve as a temporary power source during power loss events. Capacitors are often used in conjunction with voltage regulators to ensure a continuous power supply during such events, providing additional time for the device to safely shut down.

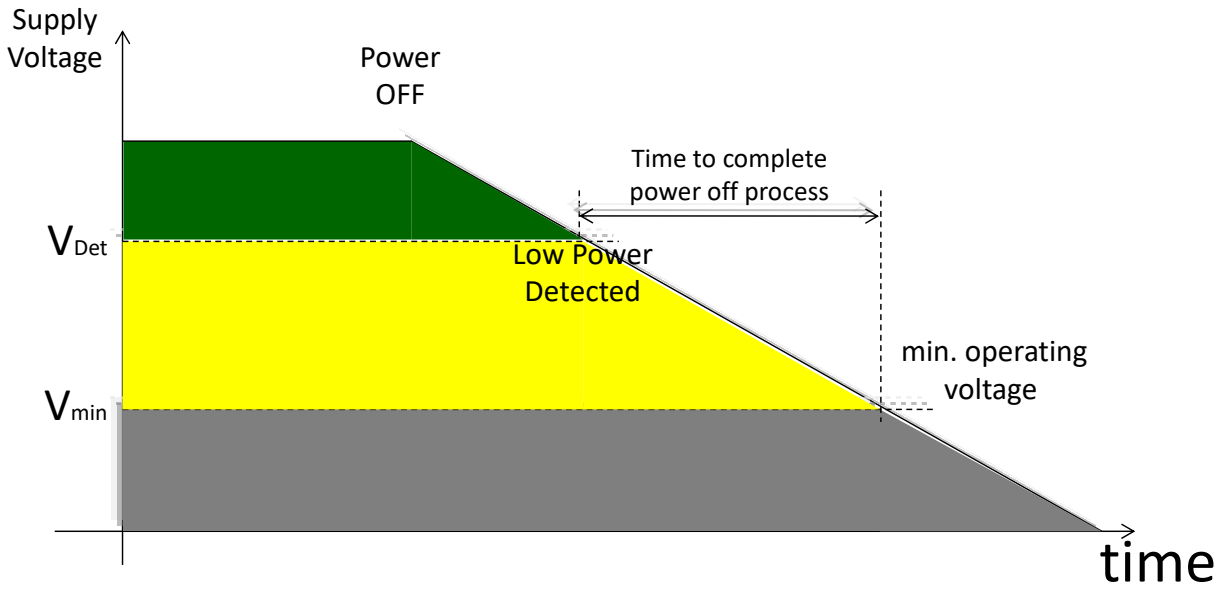

Figure 2 – Capacitors to extend operation time while power loss

Firmware Implementation

During the detection phase, the hardware components monitor the power supply and identify any changes or disruptions in the power source. The voltage detector continually monitors the input voltage, and any sudden drop or increase in voltage is detected by these hardware components.
Once a power loss event is detected, the firmware response phase is initiated. During this phase, the hardware components collaborate to ensure a gradual and safe power shutdown. This is accomplished by saving any unsaved data, immediately flushing caches, and powering off the device in a secure and controlled manner, utilizing the additional power provided by the capacitors during this process.

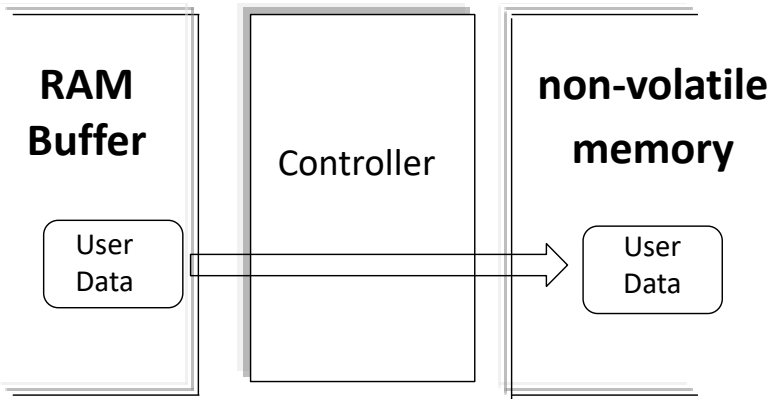

Figure 3 – Data flow while firmware response phase

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