

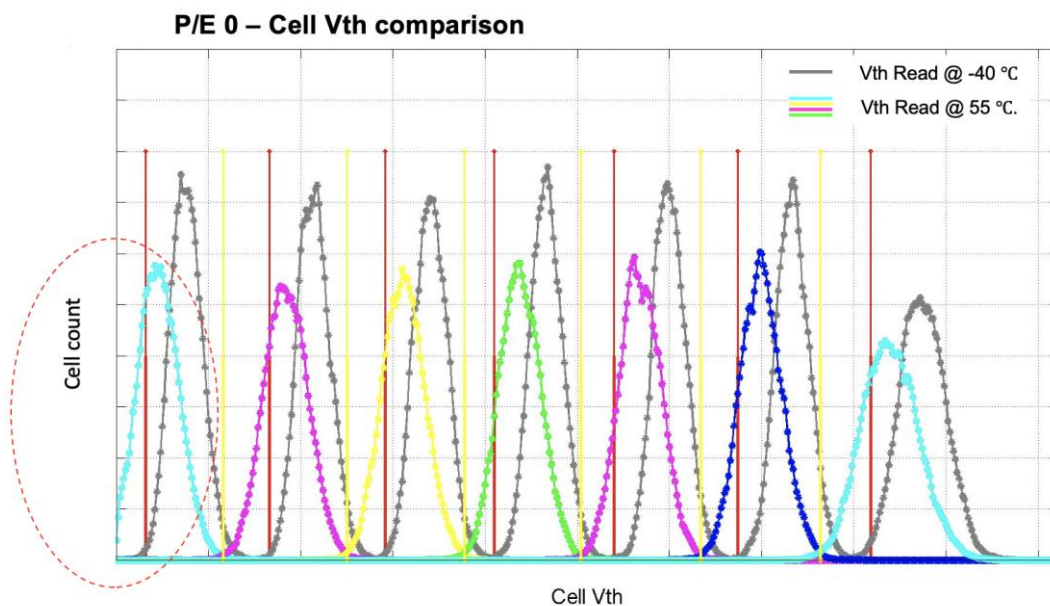
Cross Temperature Challenges in NAND Flash Technology

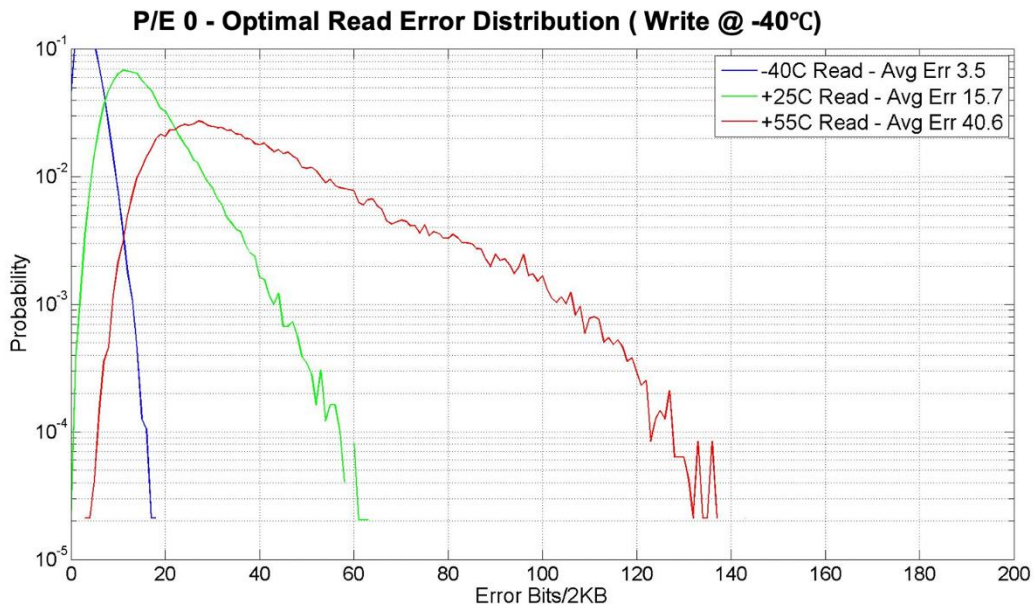
The cross-temperature effect, caused by reading and writing at different temperatures, has always presented a challenge for NAND Flash technology. Sensing data at a temperature different from that used during programming can introduce error bits, leading to unrecoverable data corruption, even when integrated error correction codes are employed. The key issue that induces these error bits is the shift in V_{th} during data sensing, and Program/Erase cycles exacerbate the problem.

When the temperature changes compared to the programming phase, V_{th} experiences a shift.

V_{th} is a critical voltage level used to read data back from the programmed data. To mitigate the issue of increased error bits during data sensing due to V_{th} shifts, recent NAND Flash designs incorporate read-level configurations.

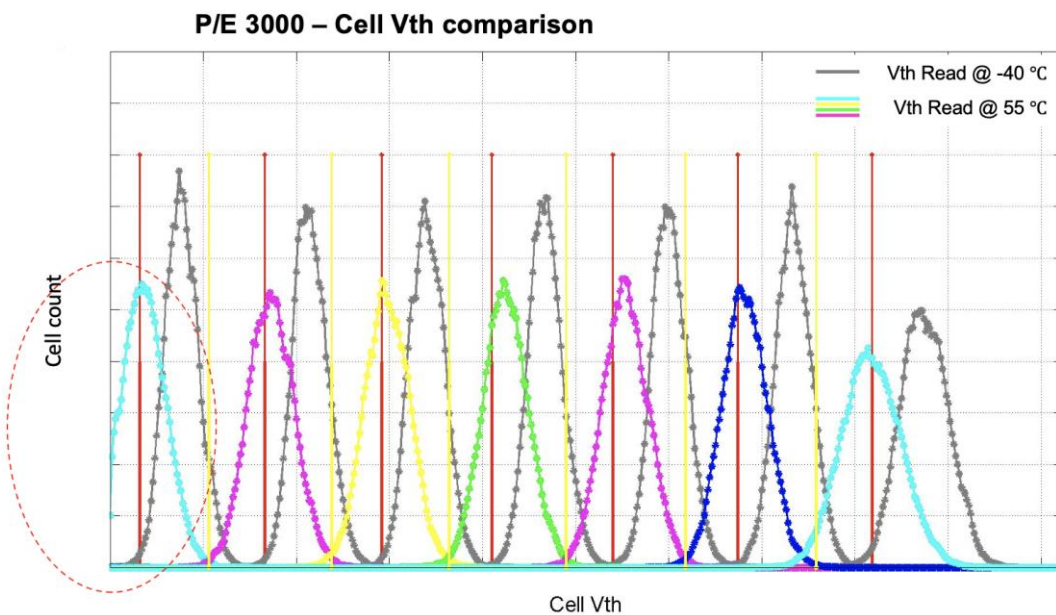
According to V_{th} distribution charts and error distribution charts, the shift impacts lower pages, but the error rate remains acceptable with both hard and soft decoders or error correction codes.

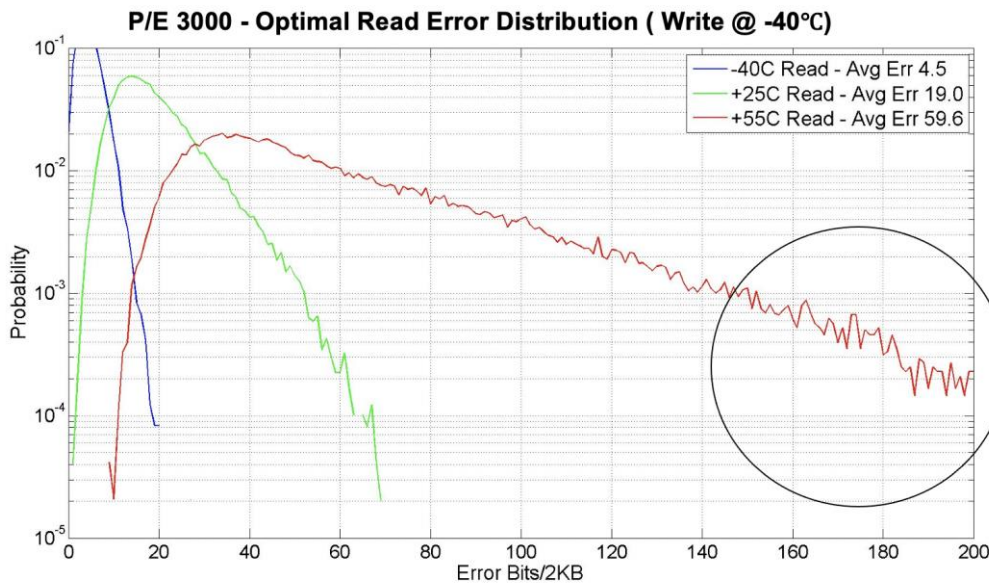




Program/Erase cycles aggravate the issue of Vth shift

However, the situation worsens after a certain number of program and erase operations are applied to the NAND Flash. This leads to a further shift towards negative voltage levels, resulting in an increase in error bits on the lower page, exceeding the error correction code's coverage range.





Some manufacturers offer screened I-temp drives based on C-temp NAND Flash and claim the same temperature performance as native I-temp NAND. While achieving the same temperature performance may be feasible, it cannot be guaranteed solely through production testing when NAND flash is in a fresh state. High-endurance conditions pose a greater challenge for cross-temperature applications. Our offer not only relies on production tests but also on NAND Flash-level research and evaluation results, validated through extensive lab testing for high-endurance conditions.

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