NAND Flash Technology

This whitepaper explains the NAND Flash Technology from the original SLC to MLC, and TLC NAND cells. A basic NAND cell (a floating gate transistor) has the capability to store a single bit. The bits represent an electrical charge which can only hold one of two values; 0 or 1. It is so, that, when the floating gate is charged, it is programmed and recognized as a binary 0. When the floating gate has no charge, it is erased and recognized as a binary value of 1.

The voltage thresholds required to store the multiple states in each of the memory technologies is demonstrated in the picture below. Not counting guard band area, each SLC state allocates 50% of the voltage range, while MLC allocates 25% and TLC 12.5%.
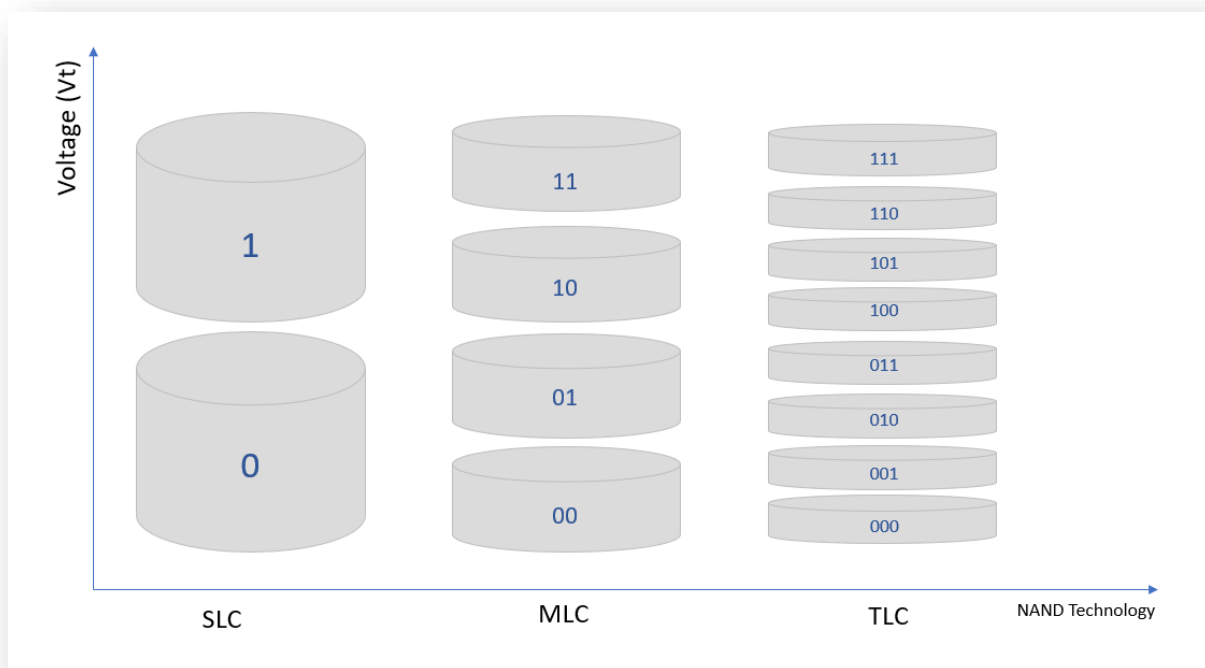

Figure 1 NAND Cell Technology

The endurance of the Flash is defined by the P/E cylces (Program/Erase cycles). Each time a block is written and erased, that is considered as 'one' cycle. It is vital to note that the cells can be written only a finite number of times. After the maximum P/E cycles are reached the Flash becomes 'Read-only.'

SLC:

Single-level cell (SLC) NAND stores a single bit of information per cell. The cell stores either a 'logic 0' or a 'logic 1', which results in the data being written and read faster. SLC provides higher performance and the highest endurance with **60,000 P/E** cycles which essentially entitles it to last longer than the other types of NAND. The guard band of voltage difference is higher as there is possibility to store one single bit, allowing the SLC Flash to have more data integrity and data retention.

However, the cost per terabyte of an SLC NAND is high and therefore not commonly used in consumer products. It is typically used for servers and other industrial applications that require speed and endurance operating on lower densities.

MLC:

Multi-level cell (MLC) NAND stores two bits per cell using 4 charge values or levels. A 2-bit MLC has a single charge level assigned to every possible combination of ones and zeros. Based on the percentage of charge in the cell, the values stored in the cell are defined. It offers around **3,000 - 5,000 P/E cycles.**

When the charge is around 25%, the cell represents a binary value of 11, when close to 50%, the cell represents a 10, when close to 75%, the cell represents a 01; and when close to 100%, the cell represents a 00. Once again, there is a region of uncertainty (read margin) between values, where the data stored in the cell cannot be precisely read MLC NAND has lower written speeds, lower number of program/erase cycles and higher power consumption compared to SLC flash memory.

TLC:

Triple-level cell (TLC) NAND stores 3 bits per cell using 8 charge values or levels. This makes the guard band between different voltage levels much less increasing the data integrity issues. However, because each cell can store 3 bits, it offers more density. A typical TLC Flash offers **3000 P/E cylces.**

The Flash cells wear off faster compared to an SLC flash as there are more charge levels whenever a Program or Erase cycle occurs.
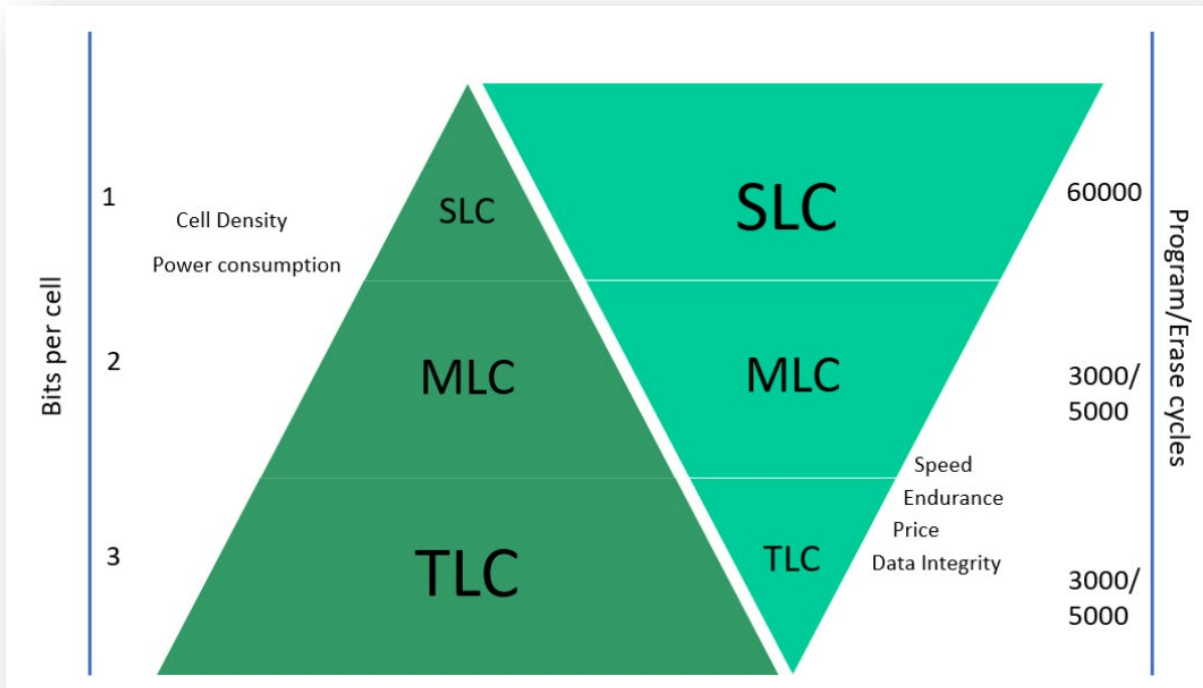
Figure 2 Flash Specifications

Pseudo mode:

Pseudo is a method of using multi-level cell (MLC), triple-level cell (TLC) in a way that reduces the number of bits stored in each cell. As explained above MLC Flash natively stores two bits per cell, TLC stores three bits per cell.

With a TLC flash, one can use the pseudo SLC mode to reduce the number of bits stored 1. This technique increases longevity of the flash and the reliability. This makes the cost per gigabyte less than that of a native SLC Flash.

For example, when a TLC Flash configured in pseudo SLC (pSLC) mode, a 10x P/E cycles of a TLC Flash can be obtained by having a third of the drive density as usable capacity.

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